



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Gilbert Wolrich et al. Art Unit: 2171  
Serial No.: 10/020,815 Examiner: Unknown  
Filed : December 12, 2001 Conf No.: 8919  
Assignee: Intel Corporation  
Title : QUEUE MANAGEMENT

Commissioner for Patents  
P.O. Box 1450  
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Technology Center 2100

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The documents are in the English language; hence no concise  
explanation is necessary per Rule 98(a)(3).

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Respectfully submitted,



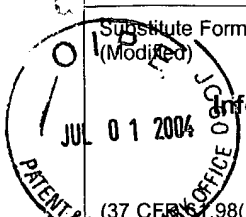
\_\_\_\_\_  
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 Substitute Form PTO-1449 (Modified) <b>Information Disclosure Statement</b> <b>by Applicant</b> (Use several sheets if necessary)	U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. 10559-614001	Application No. 10/020,815
	Applicant Gilbert Wolrich, et al.		
	Filing Date December 12, 2001	Group Art Unit 2171	

**U.S. Patent Documents**

Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	AA	09/475,614	12/30/1999	Wolrich at al.			
	AB	09/473,571	12/28/1999	Wolrich et al.			

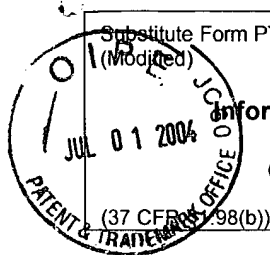
**Foreign Patent Documents or Published Foreign Patent Applications**

Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation Yes	No
	AC	WO 01/50679	07/12/2001	WIPO				
	AD	WO 01/50247	07/12/2001	WIPO				
	AE	WO 01/48619	07/05/2001	WIPO				
	AF	WO 01/48606	07/05/2001	WIPO				
	AG	WO 01/48596	07/05/2001	WIPO				
	AH	WO 01/16782	03/08/2001	WIPO				
	AI	WO 01/16770	03/08/2001	WIPO				
	AJ	WO 01/16769	03/08/2001	WIPO				
	AK	WO 01/15718	03/08/2001	WIPO				
	AL	WO 97/38372	10/16/1997	WIPO				
	AM	WO 94/15287	07/07/1994	WIPO				
	AN	EP 0 809 180	11/26/1997	Europe				
	AO	EP 0 745 933	12/04/1996	Europe				
	AP	EP 0 633 678	01/11/1995	Europe				
	AQ	EP 0 464 715	01/08/1992	Europe				
	AR	EP 0 379 709	08/01/1990	Europe				
	AS	59111533	06/27/1984	Japan			Abstract only	

**Other Documents (include Author, Title, Date, and Place of Publication)**

Examiner Initial	Desig. ID	Document
	AT	Byrd et al., "Multithread Processor Architectures," <i>IEEE Spectrum</i> , Vol. 32, No. 8, New York, 1 August 1995, pp. 38-46.
	AU	Doyle et al., <i>Microsoft Press Computer Dictionary</i> , 2 <sup>nd</sup> ed., Microsoft Press, Redmond, Washington, USA, 1994, p. 326.

Examiner Signature	Date Considered
EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	



Substitute Form PTO-1449

U.S. Department of Commerce  
Patent and Trademark Office

Attorney's Docket No.

10559-614001

Application No.

10/020,815

**Information Disclosure Statement  
by Applicant**

(Use several sheets if necessary)

Applicant

Gilbert Wolrich, et al.

Filing Date

December 12, 2001

Group Art Unit

2171T

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**Other Documents (include Author, Title, Date, and Place of Publication)**

Examiner Initial	Desig. ID	Document
	AV	Fillo et al., "The M-Machine Multicomputer," IEEE Proceedings of MICRO-28, 1995, pp. 146-156. ✓
	AW	Gomez et al., "Efficient Multithreaded User-Space Transport for Network Computing: Design and Test of the TRAP Protocol," <i>Journal of Parallel and Distributed Computing</i> , Academic Press, Duluth, Minnesota, USA, vol. 40, no. 1, 10 January 1997, pp. 103-117. ✓
	AX	Haug et al., "Reconfigurable hardware as shared resource for parallel threads," IEEE Symposium on FPGAs for Custom Computing Machines, 1998. ✓
	AY	Hauser et al., "Garp: a MIPS processor with a reconfigurable coprocessor," Proceedings of the 5 <sup>th</sup> Annual IEEE Symposium on Field-Programmable Custom Computing Machines, 1997. ✓
	AZ	Hyde, R., "Overview of Memory Management," <i>Byte</i> , vol. 13, no. 4, 1998, pp. 219-225. ✓
	AAA	Litch et al., "StrongARMing Portable Communications," IEEE Micro, 1998, pp. 48-55. ✓
	ABB	Schmidt et al., "The Performance of Alternative Threading Architectures for Parallel Communication Subsystems," Internet Document, <i>Online!</i> , 13 November 1998. ✓
	ACC	Thistle et al., "A Processor Architecture for Horizon," IEEE, 1998, pp. 35-41. ✓
	ADD	Tremblay et al., "A Three Dimensional Register File for Superscalar Processors," IEEE Proceedings of the 28 <sup>th</sup> Annual Hawaii International Conference on System Sciences, 1995, pp. 191-201. ✓
	AEE	Trimberger et al., "A time-multiplexed FPGA," Proceedings of the 5 <sup>th</sup> Annual IEEE Symposium on Field-Programmable Custom Computing Machines, 1998. ✓
	AFF	Turner et al., "Design of a High Performance Active Router," Internet Document, <i>Online</i> , 18 March 1999. ✓
	AGG	Vibhatavani et al., "Simultaneous Multithreading-Based Routers," Proceedings of the 2000 International Conference of Parallel Processing, Toronto, Ontario, Canada, 21-24 August 2000, pp. 362-359. ✓
	AHH	Wazlowski et al., "PRSIM-II computer and architecture," IEEE Proceedings, Workshop on FPGAs for Custom Computing Machines, 1993. ✓

Examiner Signature

Date Considered

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